IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: KESHAVARZI et al.	Examiner: Not yet assigned
Serial No.: Not yet assigned	Group Art Unit: Not yet assigned
Filing Date: Herewith	INTEL Docket No.: P18061
FOR: **MEMORY CELL WITHOUT HALO INPLANT**	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Applicants submit herewith patents, publications or other information of which they are aware that they believe may be material to the examination of this application, and in respect of which, there may be a duty to disclose.

The filing of this information disclosure statement shall not be construed as a representation that a thorough search has been made, an admission that the information cited is, or is considered to be, material to patentability, or that no other material information exists. Nor shall the filing of this information disclosure statement be construed as an admission against interest in any manner.

This Information Disclosure Statement is filed in accordance with 37 CFR §§1.56, 1.97 and 1.98. The items listed on the accompanying Form PTO-1449 may be deemed to be pertinent to the above-identified application and are made of record to assist the Patent and Trademark Office in its examination of this application. The Examiner is respectfully requested to fully consider the items listed on the enclosed copy of Form PTO-1449 and to independently ascertain their teaching.

No fee is believed to be due under 37 CFR §1.17(p) for this Information Disclosure Statement since it is being filed concurrently with the above-identified application.

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Respectfully submitted,

December 31, 2003
Date

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet	1	of	1

Complete if Known	
Application Numb r	Not yet assigned
Filing Date	Herewith
First Named Inventor	KESHAVARZI, Ali
Group Art Unit	Not yet assigned
Examiner Name	Not yet assigned
INTEL Docket Number	P18061

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	A	Ohsawa, Takashi et al., "Memory Design Using a One-Transistor Gain Cell on SOI, IEEE Journal of Solid-State Circuits, Vol. 37, No. 11, November 2002, ISSN: 0018-9200, pp. 1510-1522.	
	B	Thompson, Scott, et al., "MOS Scaling: Transistor Challenges for the 21st Century", Intel Technology Journal Q3'98. 19pgs.	
	C	Ohsawa, Takashi et al., "ISSCC 2002/Session 9/Dram and Ferroelectric Memories / 9.1", Memory LSI Research and Development Center, Yokohama, Japan. 3pgs.	
	D	Brand, A., "Intel's 0.25 Micron, 2.0Volts Logic Process Technology", Intel Technology Journal Q3'98. 9pgs.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Unique citation designation number. [2]Applicant is to place a check mark here if English language Translation is attached.